BCH NAND CODEC IP CORE

Specification

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Release Information

Name	BCH NAND Codec IP Core
Version	16.0
Build data	2016.2
Ordering code	ip-bch-nand-512-1k

Introduction

The BCH IP core for NAND Flash is to correct random error bits occurred in data frames. The BCH encoder generates parity bits and the BCH decoder finds & corrects error bits using three sub-modules: Error Detect Coder (EDC), Key Equation Solver (KES) and Chien Search Machine (CSM). These sub-modules are scheduled in a pipeline manner, which mean the BCH decoder can decode three data frames concurrently with each frame in each decoding stage. The KES module is optimized to get equivalent latency with other sub-modules. The CSM is implemented area efficiently using BOYUAN's proprietary technologies.

Key Features

- Supported data block: 512B, 1KB, etc.
- Support multiple ECC levels
- Configurable parallel data input width
- Configurable parallel parity output width
- Full pipelined decoder
- Report decoding results

Applications

- SLC/MLC NAND Flash
- Few serials of TLC NAND Flash

Deliverables

- RTL Verilog source code or synthesized netlist
- Full Verilog simulation environment
- Design documents

Macro Architecture

Figure 1 illustrates The BCH NAND Encoder IP Core block diagram. The BCH NAND Encoder consists of one control module (CTRL), one input interface module (IINF), one output interface module (OINF) and the datapath module (Datapath). One Linear Feedback Shift Register (LFSR) constitutes the datapath module.

Figure 2 illustrates The BCH NAND Decoder IP Core block diagram. The BCH NAND Decoder consists of one control module (CTRL), one input interface module (IINF), one internal data buffer (BUF), one output interface module (OINF), one error detection module (EDC), one key-equation solver module (KES), and one Chien search machine module (CSM).

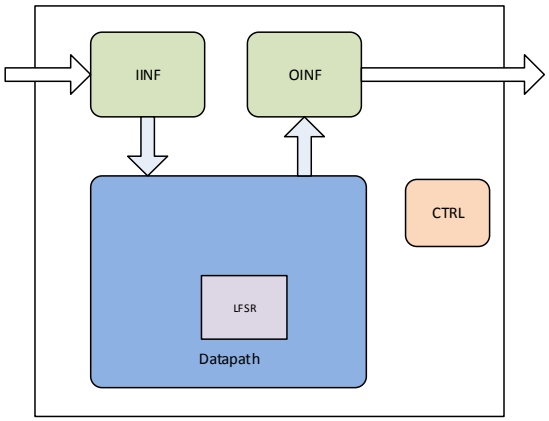

Figure 1 BCH NAND Encoder IP Core Block Diagram

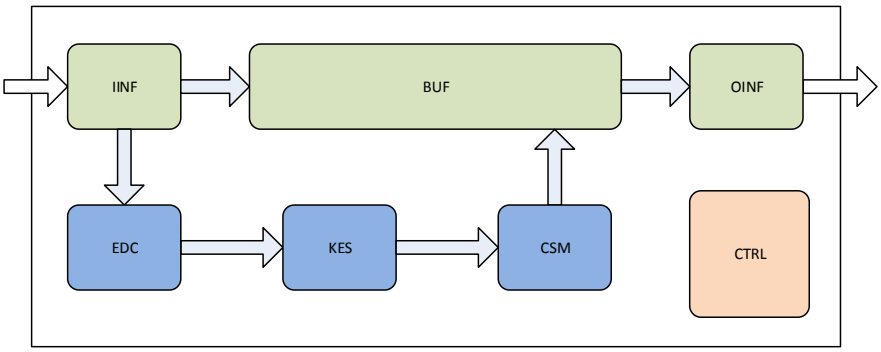

Figure 2 BCH NAND Decoder IP Core Block Diagram

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the I/O ports of The BCH NAND Encoder IP Core. The input and output interface data flow can be controlled by both sides.

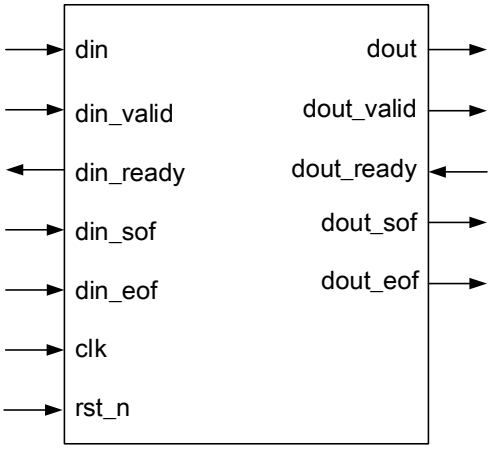

Figure 3 The BCH NAND Encoder port map

Table 1 The BCH NAND Encoder port map description

Port	Direction	Width	Description
clk	Input	1	The clock signal.
rst_n	Input	1	The reset signal. Asynchronous and active low reset.
din	Input	*BUS_WIDTH*	The input data bus. It's sampled by the Encoder Core when both din_valid and din_ready are asserted.
din_valid	Input	1	The input data valid signal. It's an active high signal.
din_ready	Output	1	The input data ready signal. It's an active high signal.
din_sof	Input	1	The input start of frame flag. It's an active high signal. It indicates the first input data of one data block.
din_eof	Input	1	The input end of frame flag. It's an active high signal. It indicates the last input data of one data block.
dout	Output	*BUS_WIDTH*	The output data bus. It should be sampled by the Encoder's integrate module when both dout_valid and dout_ready are asserted.
dout_valid	Output	1	The output data valid signal. It's an active high signal.
dout_ready	Input	1	The output data ready signal. It's an active high signal.
dout_sof	Output	1	The output start of frame flag. It's an active high signal. It indicates the first output data of one data block.
dout_eof	Output	1	The output end of frame flag. It's an active high signal. It indicates the last output data of one data block.

Figure 4 shows a graphic symbol, and Table 2 describes the I/O ports of The BCH NAND Decoder IP Core. The input and output interface data flow can be controlled by both sides.

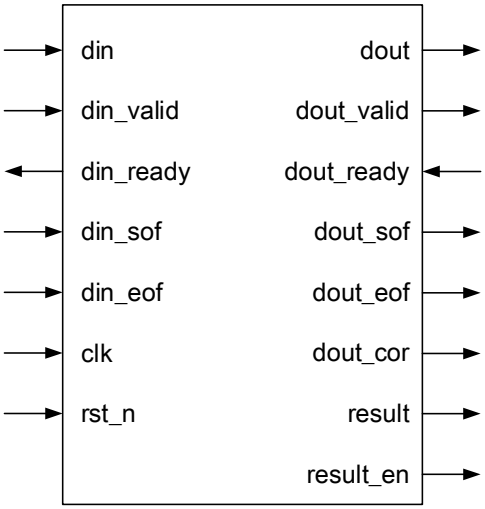

Figure 4 The BCH NAND Decoder port map

Table 2 The BCH NAND Decoder port map description

Port	Direction	Width	Description
clk	Input	1	The clock signal.
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din	Input	*BUS_WIDTH*	The input data bus. It's sampled by the Decoder Core when both din_valid and din_ready are asserted.
din_valid	Input	1	The input data valid signal. It's an active high signal.
din_ready	Output	1	The input data ready signal. It's an active high signal.
din_sof	Input	1	The input start of frame flag. It's an active high signal. It indicates the first input data of one data block.
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dout	Output	*BUS_WIDTH*	The output data bus. It should be sampled by the Decoder's integrate module when both dout_valid and dout_ready are asserted.
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dout_ready	Input	1	The output data ready signal. It's an active high signal.
dout_sof	Output	1	The output start of frame flag. It's an active high signal. It indicates the first output data of one data block.
dout_eof	Output	1	The output end of frame flag. It's an active high signal. It indicates the last output data of one data block.
dout_cor	Output	1	The output corrected flag. It's an active high signal. It indicates whether the data is corrected.
result	Output	8	The decoding result. It's an active high signal.
result_en	Output	1	The decoding result enable. The result are valid only when result_en is asserted. It's an active high signal.

Parity Length vs. ECC Levels

Table 3 and Table 4 describes the typical ECC levels of the BCH NAND IP Core for 512B and 1KB data blocks individually, with the parity byte number. The BCH decoder internal KEY component is optimized according to the selected ECC level value.

Table 3 The BCH NAND IP Core ECC Levels for 512B Data Block

ECC Level	8bit	24bit
Parity Length	13B	39B

Table 4 The BCH NAND IP Core ECC Levels for 1kB Data Block

ECC Level	8bit	24bit	32bit	40bit	48bit	72bit	96bit
Parity Length	14B	42B	56B	70B	84B	1001bit	1337bit

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options. The IP Core fully supports all Xilinx FPGA families. Table 5 and Table6 summarizes the BCH NAND Encoder and Decoder IP Core measurement results respectively with 8bit bus width (*BUS_WIDTH* = 8). The throughput is estimated based on 200MHz clock frequency, the actual implementation frequency depends on the final resource usage of the IP integration system.

Table 5 The BCH NAND Encoder performance

IP Core parameters		FPGA type			
		Resource		Frequency and Throughput	
DATA_BLOCK	512B	xc7k325tffg900-2L			
		LUT	374	Typical Frequency	
ECC_LEVEL	24bit	FF	338	Frequency	200MHz
		BRAM	-	Throughput	MB/s
DATA_BLOCK	1kB	xc7k325tffg900-2L			
		LUT	214	Typical Frequency	
ECC_LEVEL	8bit	FF	138	Frequency	200MHz
		BRAM	-	Throughput	MB/s
DATA_BLOCK	1kB	xc7k325tffg900-2L			
		LUT	406	Typical Frequency	
ECC_LEVEL	24bit	FF	362	Frequency	200MHz
		BRAM	-	Throughput	MB/s
DATA_BLOCK	1kB	xc7k325tffg900-2L			
		LUT	611	Typical Frequency	
ECC_LEVEL	40bit	FF	586	Frequency	200MHz
		BRAM	-	Throughput	MB/s
DATA_BLOCK	1kB	xc7k325tffg900-2L			
		LUT	1553	Typical Frequency	
ECC_LEVEL	96bit	FF	1364	Frequency	200MHz
		BRAM	-	Throughput	MB/s

Table 6 The BCH NAND Decoder performance

IP Core parameters		FPGA type			
		Resource		Frequency and Throughput	
DATA_BLOCK	512B	xc7k325tffg900-2L			
		LUT	6021	Typical Frequency	
ECC_LEVEL	24bit	FF	4257	Frequency	200MHz
		BRAM	3.5	Throughput	MB/s
DATA_BLOCK	1kB	xc7k325tffg900-2L			
		LUT	2565	Typical Frequency	
ECC_LEVEL	8bit	FF	1901	Frequency	200MHz
		BRAM	2.5	Throughput	MB/s
DATA_BLOCK	1kB	xc7k325tffg900-2L			
		LUT	5809	Typical Frequency	
ECC_LEVEL	24bit	FF	4334	Frequency	200MHz
		BRAM	2.5	Throughput	MB/s
DATA_BLOCK	1kB	xc7k325tffg900-2L			
		LUT	7486	Typical Frequency	
ECC_LEVEL	40bit	FF	4201	Frequency	200MHz
		BRAM	4.5	Throughput	MB/s
DATA_BLOCK	1kB	xc7k325tffg900-2L			
		LUT	24090	Typical Frequency	
ECC_LEVEL	96bit	FF	16271	Frequency	200MHz
		BRAM	10.5	Throughput	MB/s

Interface Timing Description

As Figure 5 depicted, for input data interface, the bus data *din* are sampled only when *din_valid* and *din_ready* are both active (clock cycle 3 and 5 in Figure 5). The output interface has similar timing as showed in Figure 6. The input and output data interface both have valid/ready handshake timing. For the Encoder Core, the input data is message word and the output data is message and parity word. For the Decoder Core, the input data is the raw data byte and the output data is the decoded message.

Figure 7 illustrates the Decoder Core's decoding result interface timing. The decoding result signal *result* are valid only when *result_en* is active. The decoding results are provided in the same order as the input frames.

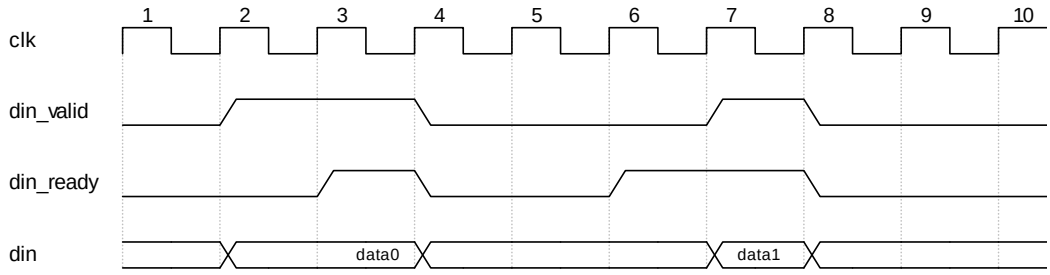

Figure 5 The BCH NAND Encoder/Decoder Input Interface Timing diagram

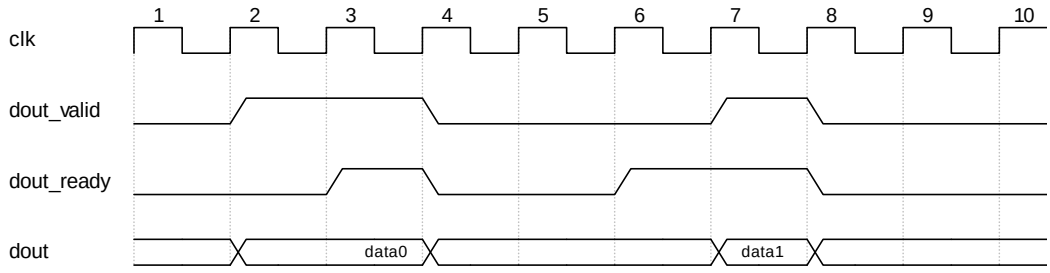

Figure 6 The BCH NAND Encoder/Decoder Output Interface Timing diagram

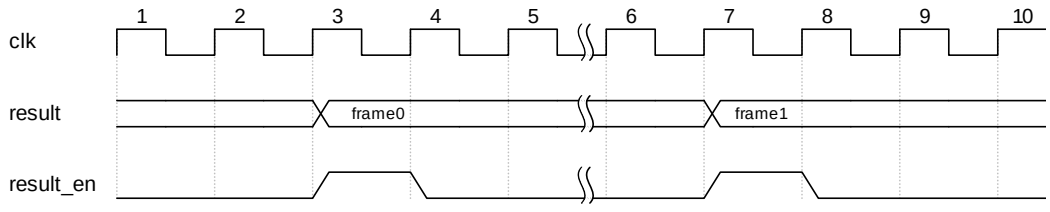

Figure 7 The BCH NAND Decoder Result Interface Timing diagram

Simulation and FPGA Test

The BCH NAND Codec IP Core contains a full simulation environment. Figure 8 illustrates the block diagram of the simulation environment. The BCH Wrap module contains Encoder and Decoder. The BCH Testbench module contains Random Number Generator, Random/Scatter Error Generator, Channel and Control & Statistics.

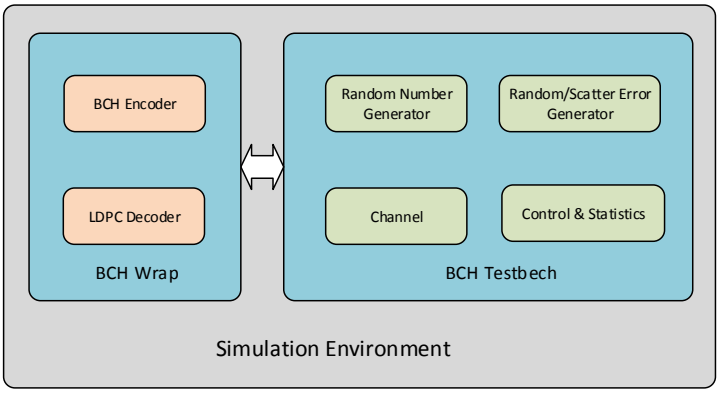

Figure 8 The BHC NAND Codec Simulation environment block diagram

Upgrade and Technical Support

Free remote technical support is provided for 12 months, includes consultation via phone and E-mail. The maximum time for processing a request for technical support is three business days.

For up-to-data information on the IP Core visit this web page:
www.bjbytech.com/id/ip_nand_bch_512_1k.html

Feedback

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Revision History

Version	Data	Changes
16.0	2016.02	Update BCH NAND interface
14.0	2014.05	Original release