LDPC NAND CODEC IP CORE

Specification

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Release Information

Name	LDPC NAND Codec IP Core
Version	18.0
Build data	2018.02
Ordering code	ip-ldpc-nand-2k-90r

Introduction

The IP core implements Boyuan's NAND Flash LDPC (18176, 16384) algorithm. The code belongs to irregular QC LDPC codes and has large girth 8. The LDPC NAND Codec IP core are highly configurable. The IP user can configure the IP Core to meet their NAND Flash system design trade-offs among the BER performance, the I/O throughput and the implementation complexity.

Key Features

- Parameterized input/output data width
- Parameterized internal LLR symbol width
- Early decoding iteration stop detection unit
- Parameterized number of node process unit for layered decoder
- Dynamic scale factor for Min-Sum decoding

Applications

- TLC NAND Flash
- Novel 3D NAND Flash

Deliverables

- RTL Verilog source code or synthesized netlist
- Full Verilog simulation environment
- Test example for Xilinx Kintex7 FPGA board
- Design documents

Macro Architecture

Figure 1 illustrates The LDPC NAND Encoder IP Core block diagram. The LDPC NAND Encoder consists of one control module (CTRL), one input data buffer (IBUF), one output data buffer (OBUF), one encoder ROM (ROM) and the datapath module (Datapath). Multiple Shift Register Adder Accumulators (SRAAs) are cascaded to constitute the datapath module.

Figure 2 illustrates The LDPC NAND Decoder IP Core block diagram. The LDPC NAND Decoder consists of one control module (CTRL), one input data buffer (IBUF), one internal LLR data buffer (BUF), one output shift register (OSR), one output data buffer (OBUF), one address/data router module (ROUTER), one parity check information module (PCM), one on-fly syndrome check module (SYN), one decoder ROM (ROM) and the node process array module (NPA). The NPA consists of multiple node process unit modules (NPUs).

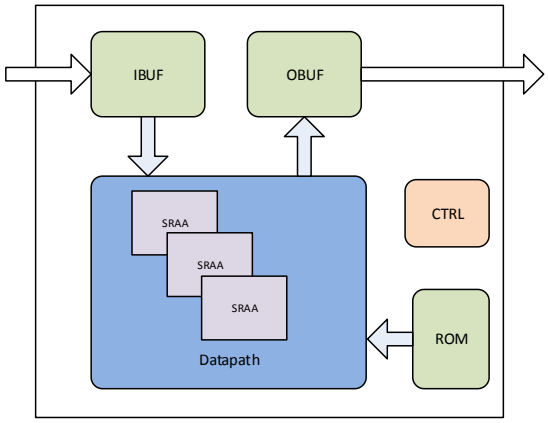


Figure 1 LDPC NAND Encoder IP Core Block Diagram

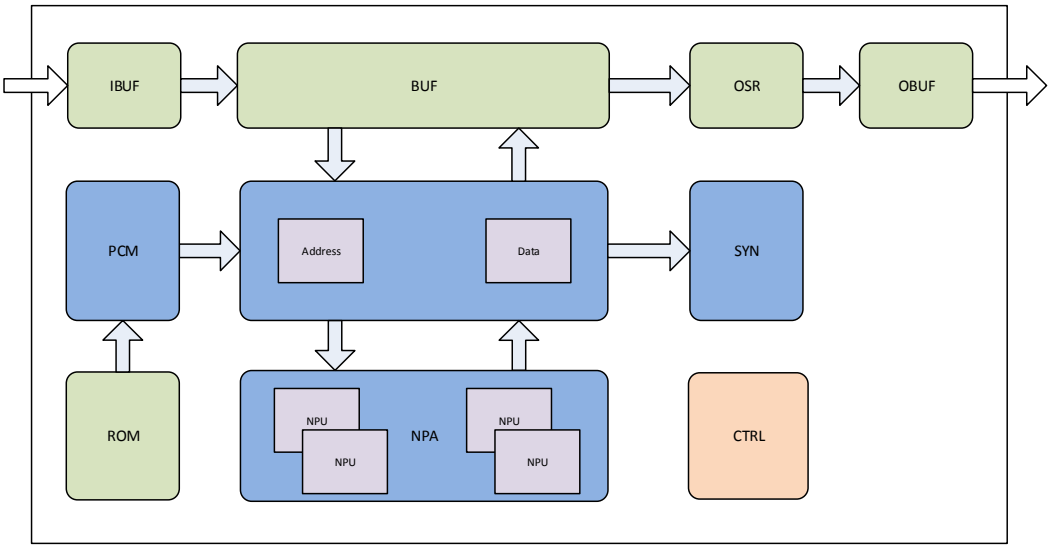


Figure 2 LDPC NAND Decoder IP Core Block Diagram

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the I/O ports of The LDPC NAND Encoder IP Core. The input and output interface data flow can be controlled by both sides.

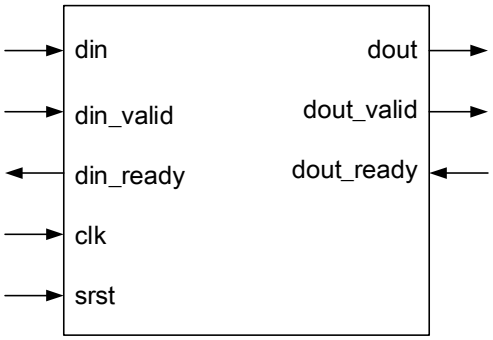


Figure 3 The LDPC NAND Encoder port map

Table 1 The LDPC NAND Encoder port map description

Port	Direction	Width	Description
clk	Input	1	The clock signal. All the IP Core's registers are operated on the rising edge of clk.
srst	Input	1	The reset signal. It's a synchronous and active high reset. The reset signal should remain active for several cycles before encoding.
din	Input	*BUS_WIDTH*	The input data bus. It's sampled by The LDPC Encoder Core when both din_valid and din_ready are asserted.
din_valid	Input	1	The input data valid signal. It's an active high signal.
din_ready	Output	1	The input data ready signal. It's an active high signal.
dout	Output	*BUS_WIDTH*	The output data bus. It should be sampled by The LDPC Encoder's integrate module when both dout_valid and dout_ready are asserted.
dout_valid	Output	1	The output data valid signal. It's an active high signal.
dout_ready	Input	1	The output data ready signal. It's an active high signal.

Figure 4 shows a graphic symbol, and Table 2 describes the I/O ports of The LDPC NAND Decoder IP Core. The input and output interface data flow can be controlled by both sides.

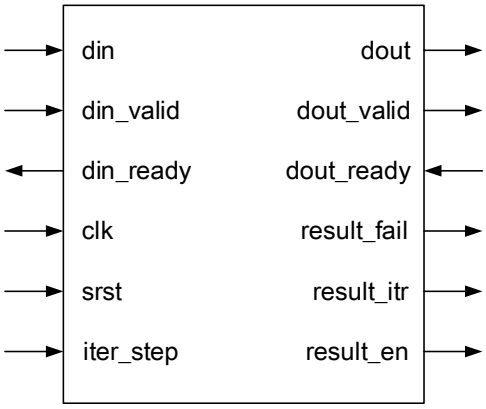


Figure 4 The LDPC NAND Decoder port map

Table 2 The LDPC NAND Decoder port map description

Port	Direction	Width	Description
clk	Input	1	The clock signal. All the IP Core's registers are operated on the rising edge of clk.
srst	Input	1	The reset signal. It's a synchronous and active high reset. The reset signal should remain active for several cycles before decoding.
din	Input	*DIN_WIDTH*	The input data bus. It's sampled by The LDPC Decoder Core when both din_valid and din_ready are asserted.
din_valid	Input	1	The input data valid signal. It's an active high signal.
din_ready	Output	1	The input data ready signal. It's an active high signal.
dout	Output	*BUS_WIDTH*	The output data bus. It should be sampled by The LDPC Decoder's integrate module when both dout_valid and dout_ready are asserted.
dout_valid	Output	1	The output data valid signal. It's an active high signal.
dout_ready	Input	1	The output data ready signal. It's an active high signal.
iter_step	Input	4	The iteration step configuration for check node process.
result_fail	Output	1	The decoding fail flag. It's an active high signal.
result_itr	Output	8	The decoding iteration counter. It indicates the decoding iteration round.
result_en	Output	1	The decoding result enable. The result_fail and result_itr are valid only when result_en is asserted. It's an active high signal.

Parameters

Table 3 describes the LDPC NAND Encoder IP Core parameters, which must be set before simulation and synthesis. Table 4 describes the LDPC NAND Decoder IP Core parameters, which must be set before simulation and synthesis.

Table 3 The LDPC NAND Encoder IP Core parameters

Parameter	Value	Description
BUS_WIDTH	8, 16, 32	The Encoder IP Core data input and output width. Using larger width of data bus increases the encoding throughput but also increases the implementation resource usage. The Encoder SRAA width is equivalent to this parameter.

Table 4 The LDPC NAND Decoder IP Core parameters

Parameter	Value	Description
QNT_BIT	3~8	The Decoder IP Core LLR input symbol width. Using larger symbol width increases the accuracy of the LLR value but also increases the implementation resource usage.
LLR_BIT	4~10	The Decoder IP Core internal LLR symbol width. Using larger symbol width increases the accuracy of the LLR value during each iteration but also increases implementation resource. The parameter LLR_BIT must not less than the parameter QNT_BIT.
PAR_DGR	2,4,8	The Decoder IP Core decoding parallel factors. It indicates how many NPUs are used in the NPA module. Using larger parallel factor increases decoding throughput but also increase the implementation resource usage.
BUS_WIDTH	8, 16, 32	The Decoder IP Core data input and output width. The data width should be configured to avoiding I/O throughput bottleneck when configuring large *PAR_DGR* parameter. The LLR bit width *DIN_WIDTH* equals to *QNT_BIT* BUS_WIDTH.* It's recommended to be configured as default value: 32.

Memory

The LDPC NAND Codec IP uses a large types of Memory, including FIFO, RAM and ROM, as introduced in Macro Architecture Figure 2 and Figure 3.

For the interface FIFOs, their data width should coincident to the external data width and the internal data width. Spatially the Decoder FIFO depth should set to deposit at least two data frames (512 LLRs) for ping-pang buffering operation, as depicted in Table 5.

Table 6 lists the LDPC NAND IP Core ROMs characterization. It should be noticed that the ROM width-depth arrangement depends on the configuration of the parameter *BUS_WIDTH*.

Table 7 lists the LDPC NAND IP Core RAMs characterization. The first RAM stores the internal APP LLR messages and its width/depth and used instance depends on the configuration of the parameter *PAR_DGR*. The second RAM stores the internal check to variable node LLR messages and its width/depth also depends on the configuration of the parameter *PAR_DGR*

Table 5 The LDPC NAND IP Core FIFO list

FIFO	Width		Depth	Instance
ldpc_enc_ififo	*BUS_WIDTH*		>16	1
ldpc_enc_ofifo	*BUS_WIDTH*		>16	1
ldpc_dec_ififo	Write	*BUS_WIDTH*QNT_BIT*	>256; 512 for best performance	71
	Read	*PAR_DGR*QNT_BIT*		
ldpc_dec_ofifo	Write	256	>64; 128 for best performance	1
	Read	*BUS_WIDTH*		

Table 6 The LDPC NAND IP Core ROM list

ROM	Width	Depth	Instance
ldpc_enc_rom	*BUS_WIDTH* *7	16384/ *BUS_WIDTH*	1
ldpc_dec_rom	31	56	1
ldpc_dec_mh	9	56	1

Table 7 The LDPC NAND IP Core RAM list

RAM	Width	Depth	Instance
ldpc_ram_dist	*LLR_BIT*	256/*PAR_DGR*	*PAR_DGR*71
ldpc_ram_blk	*PAR_DGR*QNT_BIT*31	(256*7)/ *PAR_DGR*	1

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options. The IP Core fully supports all Xilinx FPGA families. Table 8 and Table9 summarizes the LDPC NAND Encoder and Decoder IP Core measurement results respectively. The throughput is estimated based on 200MHz clock frequency, the actual implementation frequency depends on the final resource usage of the IP integration system.

Table 8 The LDPC NAND Encoder performance

IP Core parameters		FPGA type			
		Resource		Frequency and Throughput	
BUS_WIDTH	32	xc7k325tffg900-2L			
		LUT	26k	Typical Frequency	
		FF	5k	Frequency	200MHz
		BRAM	3.5	Throughput	800MB/s
BUS_WIDTH	16	xc7k325tffg900-2L			
		LUT	13k	Typical Frequency	
		FF	5k	Frequency	200MHz
		BRAM	3.5	Throughput	400MB/s

Table 9 The LDPC NAND Decoder performance

IP Core parameters		FPGA type			
		Resource		Frequency and Throughput	
QNT_BIT	6	xc7k325tffg900-2L			
LLR_BIT	6	LUT	49k	Typical Frequency, 2 iteration	
PAR_DGR	8	FF	40k	Frequency	200MHz
BUS_WIDTH	32	BRAM	22	Throughput	800MB/s
QNT_BIT	6	xc7k325tffg900-2L			
LLR_BIT	6	LUT	35k	Typical Frequency, 2 iteration	
PAR_DGR	4	FF	29k	Frequency	200MHz
BUS_WIDTH	32	BRAM	11	Throughput	400MB/s

Interface Timing Description

As Figure 5 depicted, for input data interface, the bus data *din* are sampled only when *din_valid* and *din_ready* are both active (clock cycle 3 and 5 in Figure 5). The output interface has similar timing as showed in Figure 6. The input and output data interface both valid/ready handshake timing. For the Encoder Core, the input data is message word and the output data is message and parity word. For the Decoder Core, the input data is the LLR symbols and the output data is the decoded message.

Figure 7 illustrates the Decoder Core's decoding result interface timing. The decoding fail flag *result_fail* and iteration counter *result_itr* are valid only when *result_en* is active. The decoding results are provided in the same order as the input frames.

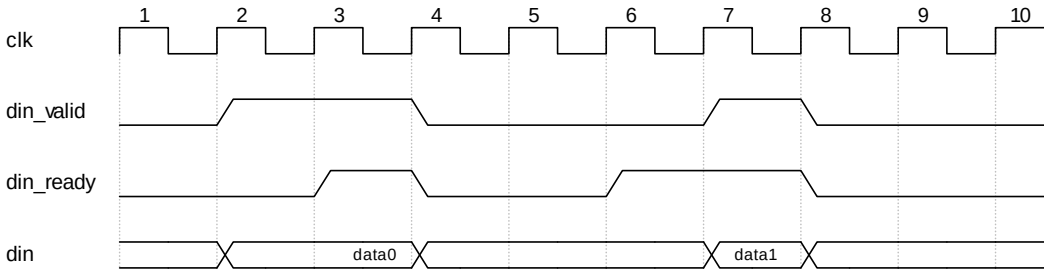


Figure 5 The LDPC NAND Encoder/Decoder Input Interface Timing diagram

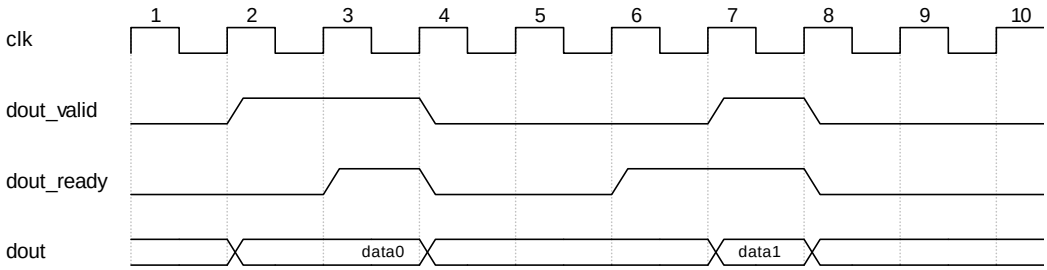


Figure 6 The LDPC NAND Encoder/Decoder Output Interface Timing diagram

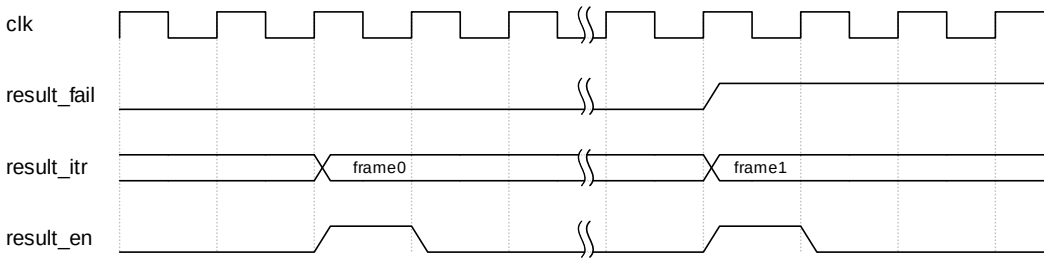


Figure 7 The LDPC NAND Decoder Result Interface Timing diagram

Simulation and FPGA Test

The LDPC NAND Codec IP Core contains a full simulation/test environment. Figure 8 illustrates the block diagram of the Xilinx FPGA test environment. The LDPC Test Wrap module contains Encoder and Decoder core with other noise generator, channel and statistics modules. The LDPC Test Wrap module are used both in simulation environment and FPGA test environment.

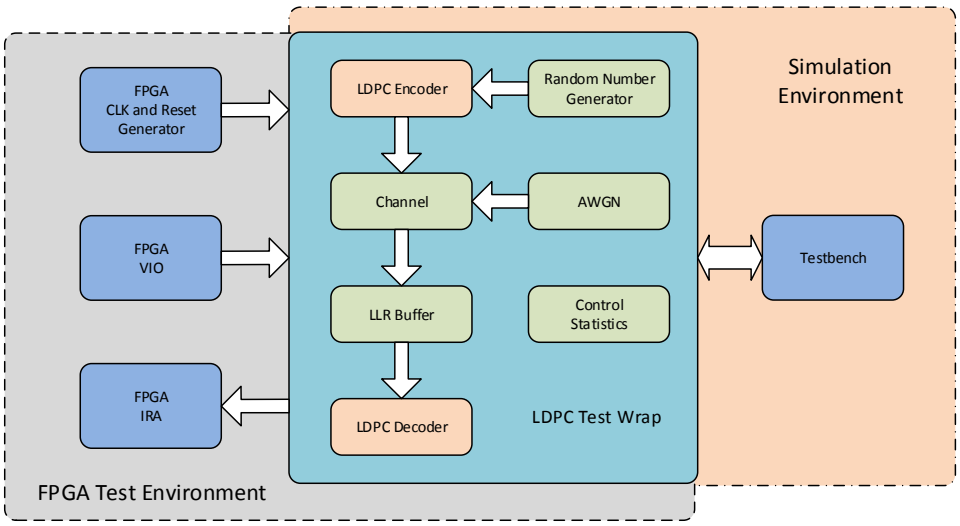
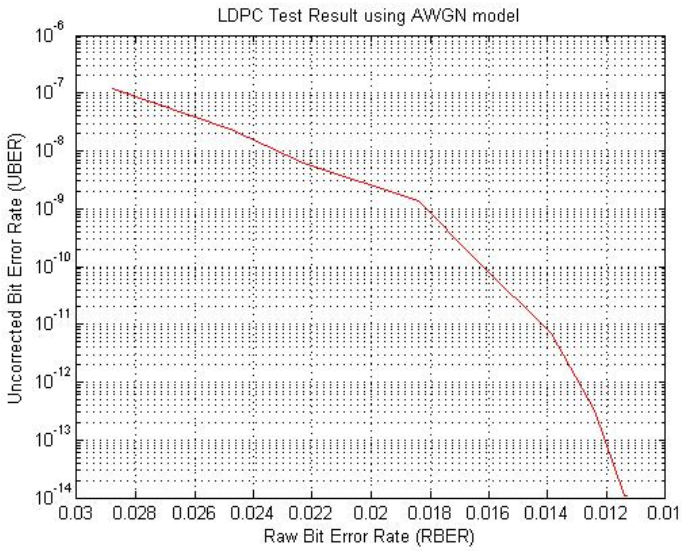


Figure 8 The LDPC NAND Codec Simulation and Test environment block diagram

For FPGA Test, the CLK and Reset Generator provides clock source and does initial system reset. The VIO module changes SNR for AWGN in the LDPC Test Wrap. The IRA collects all available decoding statistics signals to be observed, including tested frames, error frames and iteration counter, etc. The user can set up the test in their own FPGA board in few minutes through update constraints file and the top level corresponding Xilinx IP Cores. Figure 9 depicts the actual FPGA test result of the Decoder RBER-UBER performance using AWGN noise channel model when both input and internal LLR symbol is configured to 6 bits.



- Figure 9 The LDPC NAND Decoder RBER-UBER performance

Upgrade and Technical Support

Free remote technical support is provided for 12 months, includes consultation via phone and E-mail. The maximum time for processing a request for technical support is three business days.

For up-to-data information on the IP Core visit this web page:
www.bjbytech.com/id/ip_nand_ldpc_2k_90r.html

Feedback

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Revision History

Version	Data	Changes
18.0	2018.02	Update LDPC NAND algorithm
17.0	2017.05	Original release